

Compal Confidential

HH514 SUB Schematic Document

LS-L971P

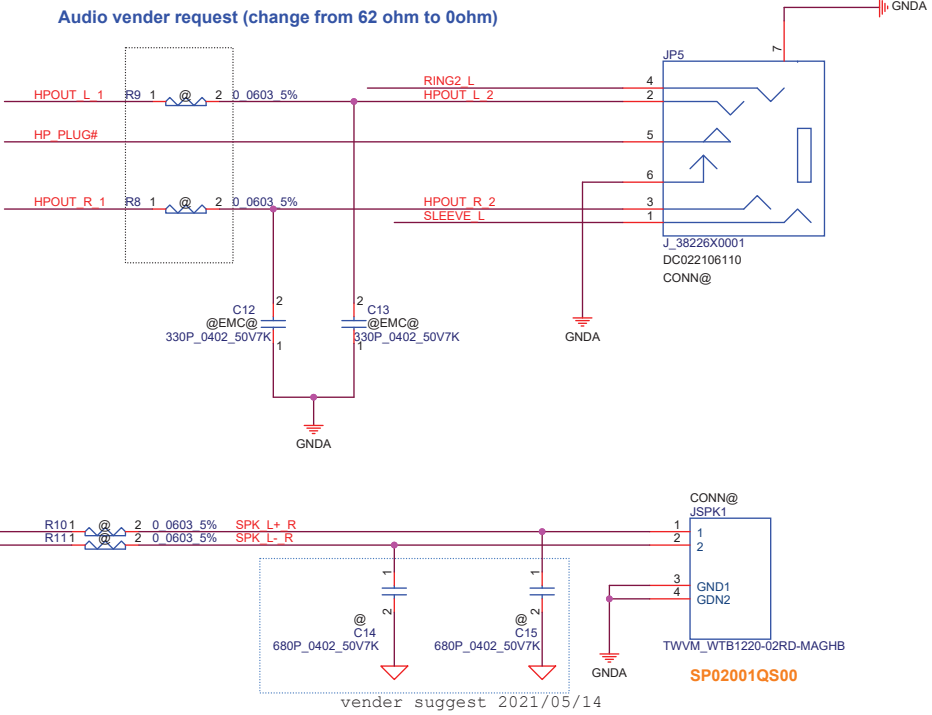
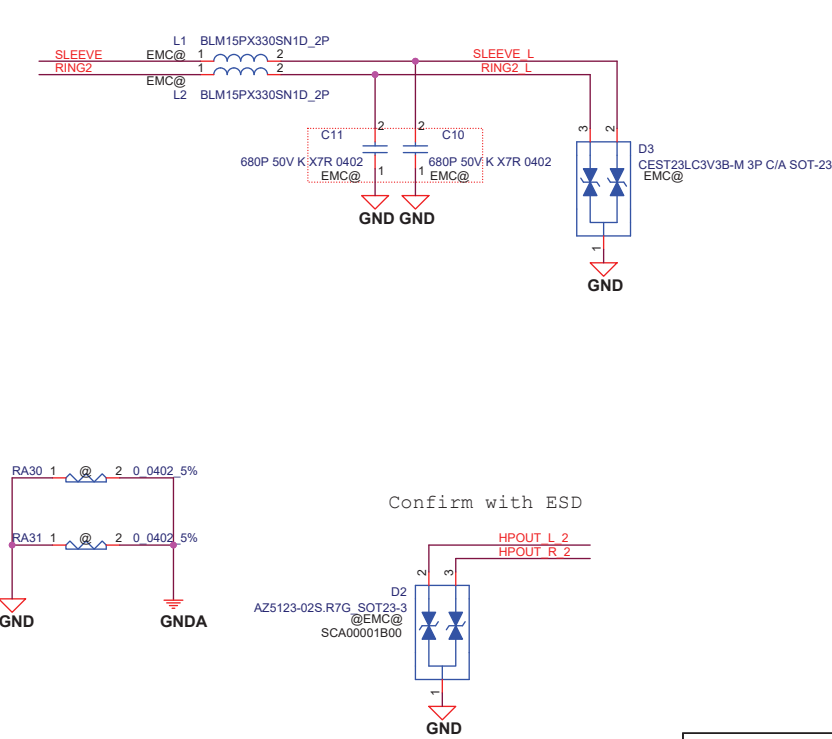
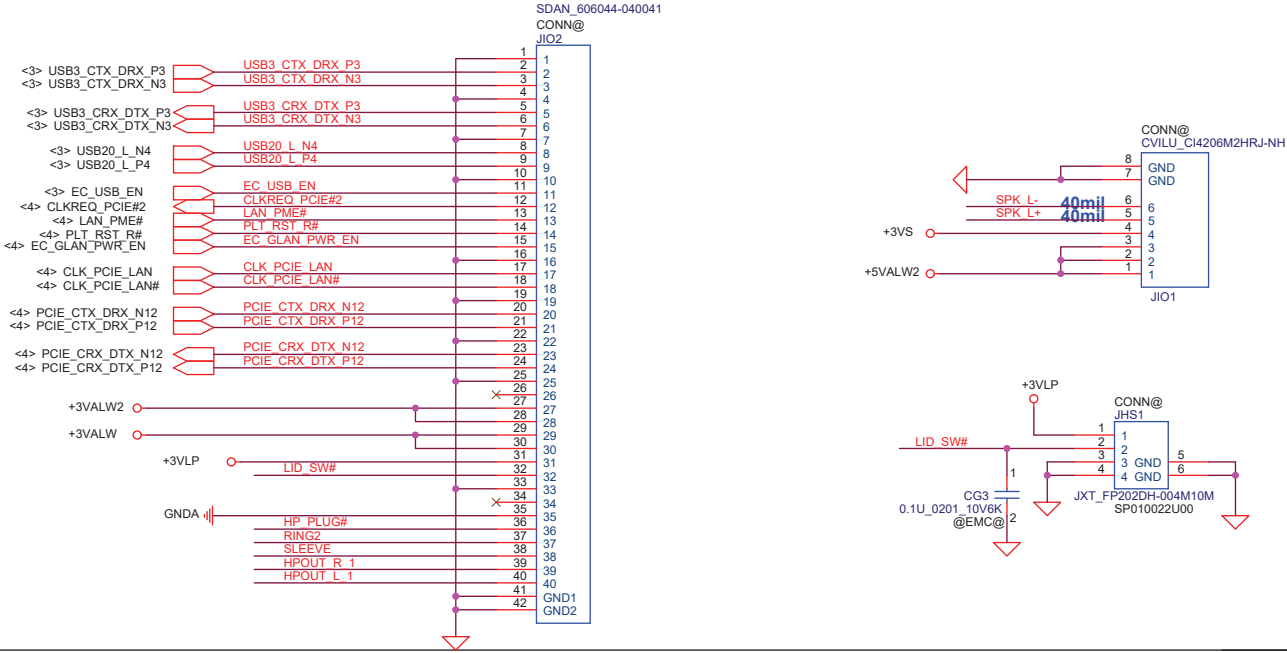
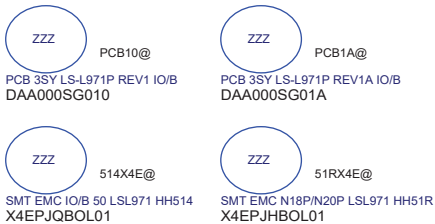
Rev: 1.A

2021-11-24

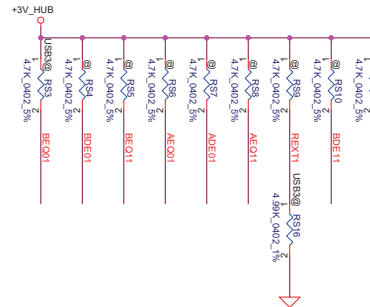
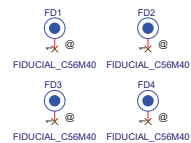
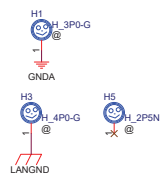
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Issued Date	2021/11/24	Deciphered Date	2024/11/24	Title	Cover Sheet
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				HH514 LS-L971P IO Board	1.A
				Date: Wednesday, November 24, 2021	Sheet 1 of 5

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MODEL NAME: HH514  
PCB NAME: LS-L971P IO/B  
COMPAL P/N:  
REVISION: 1.A  
DATE: 2021/11/24



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2024/11/24		Title		IO CONN & LED & Audio Jack	
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Date		Wednesday, November 24, 2021		Sheet 2 of 5	
Model Name		HH514 LS-L971P IO Board		Rev 1.A	

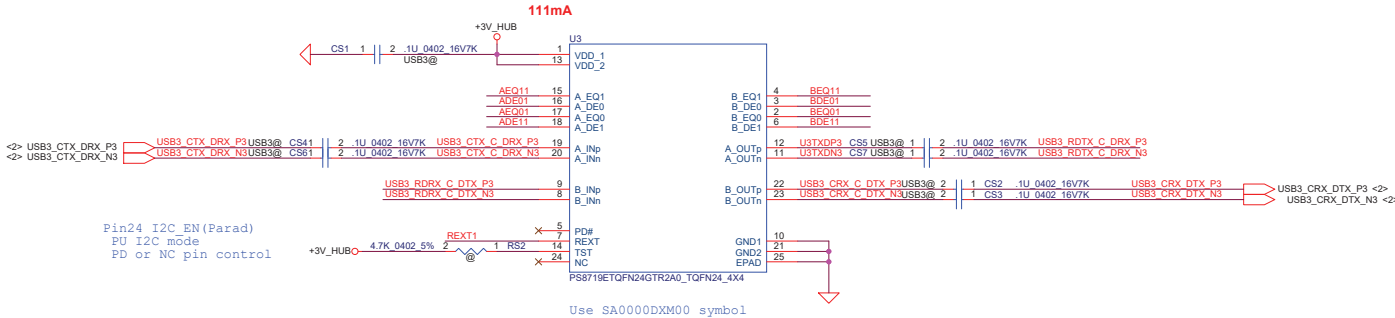


[A\_EQ1,A\_EQ0] [B\_EQ1,B\_EQ0] -> (for chanel A and B)  
 LL EQ for channel loss up to 9.5dB(default)  
 LH EQ for channel loss up to 13dB  
 HL EQ for channel loss up to 4.5dB  
 HH EQ for channel loss up to 7.5dB

[A\_DE1,A\_DE0] [B\_DE1,B\_DE0] -> (for chanel A and B)  
 LL 3.5dB de-emphasis  
 LH No de-emphasis  
 HL 2.7dB de-emphasis  
 HH 5dB de-emphasis

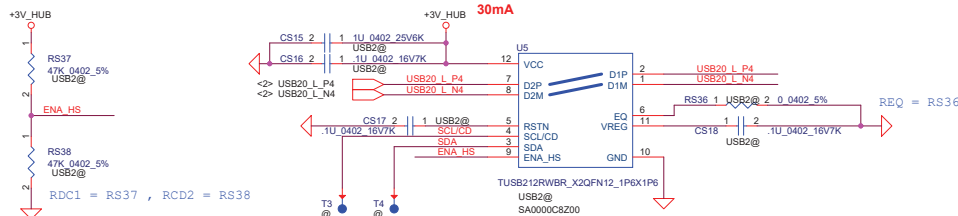
RS11 to Tuning Vswing  
 Default = 4.99K  
 RS11 can use 2.5K to 10K

EQ and DE chanel are Internally Pull down at ~150K(Parad)

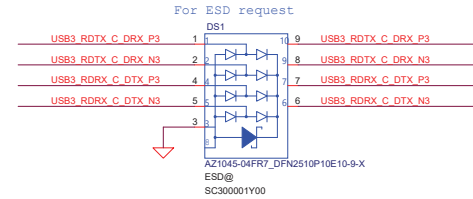
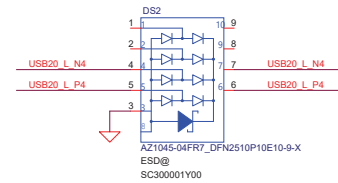


Pin24 I2C\_EN(Parad)  
 PU I2C mode  
 PD or NC pin control

Use SA0000DXM00 symbol



Use SA0000C8Z00 symbol



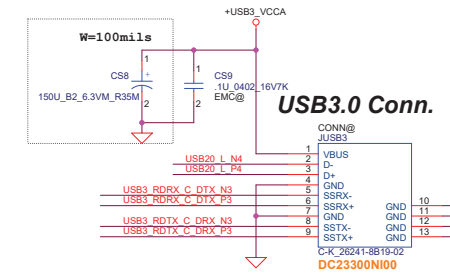
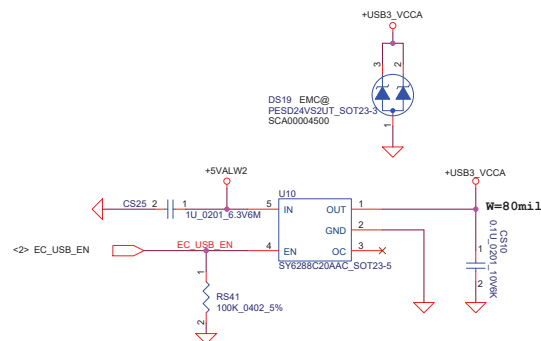
EQ pin REQ = RS36

	REQ	Level	
AC Boost	0 Ω	0	AC Boost Level 2: REQ = 3.83 K
	1.69 k ±1%	1	
	3.83 k ±1%	2	
	DNI	3	

ENA\_HS pin RDC1 = RS37, RDC2 = RS38

	PARAMETER	VALUE	
DC Boost	RDC1	22 kΩ - 47 kΩ	Mid DC Level: RDC1 = DNI RDC2 = DNI
	RDC2	Do Not Install (DNI)	
	Level	40 mV Low DC Boost	
	DNI	DNI	
	DNI	22 kΩ - 47 kΩ	80 mV High DC Boost

Pull-down and pull-up (to 3.3 V) resistors for DC\_BOOST pins must be between 22 kΩ to 47 kΩ in non I2C mode.



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Issued Date	2021/11/24	Deciphered Date
Deciphered Date	2024/11/24	Title
		USB3/USB2 Redriver
		Document Number
		HH514 LS-L971P IO Board
		Rev 1A
		Date: Wednesday, November 24, 2021   Sheet 3 of 5

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From EC
High active.
EN threshold voltage min:1.2V
typ:1.6V max:2.0V
Current limit threshold 1.5-2.8A
+3V_LAN Rising time must >0.5ms and <100ms

```

W=60mil

+REGOUT

1

2

CL1 LDO02  
0.1uF 0201 10V/6K

10V

**C16**  
0.1u 2001 100/0K  
Place near Pin 3,8,30

**C17**  
0.1u 2001 100/0K  
Place near Pin 22

**C18**  
0.1u 2001 100/0K  
Place near Pin 22

**C19**  
1u 2001 6.3/63M  
Place near Pin 22

3.3V 65mA  
1V 150mA

Place near Pin 11

Place near Pin 32

P/N: SJ10000UP00 S CRYSTAL 25MHZ 10PF XRCGB25M000F2P34R0)

LAN LED0

XTLO

XTLI

LAN LED2

XTLO

XTLI

LAN GPO remove, default is LED but FH51M not support

24 +REGOUT

23 +3V\_LAN

22 +LAN\_VDD

21 LAN\_PME#\_R

20 ISOLATE#

19 PLT\_RST\_R#

18 PCIE\_CRX\_RD\_C.DTX\_N12

17 PCIE\_CRX\_RD\_C.DTX\_P12

0 0A502 5% 1

2 RL4

1 RL6

0+3V\_LAN

LAN\_PME# <->

reserve EC\_LAN\_PME# pull high 47K to +3VLP\_EC

PLT\_RST\_R# <->

300CXTF18

00-CG\_0FN32\_444

CLK\_PCIE\_LAN <->

CLK\_PCIE\_LAN# <->

CXTX\_RD\_C.DRX\_N12

CXTX\_RD\_C.DRX\_P12

CLKREQ\_PCIE#2 pull up at PCH side

[illegible]

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Revision	1A		Date	2024/11/24

Item	Page #	Title	Date	Request Owner	Issue Description	Solution Description	Rev.

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				HH514 LS-L971P IO Board		1.A
Date: Wednesday, November 24, 2021				Sheet 5 of 5		